Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (withdrawn): A semiconductor memory device comprising:

a silicon layer having a first diffused region and a second diffused region formed therein;

a gate electrode formed through an insulating film on one side of the silicon layer between the first and the second diffused regions;

a capacitor formed on said one side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said one side of the silicon layer and connected to the second diffused region;

and a scrapping word line formed on the other side of the silicon layer and connected to the gate electrode.

3. (canceled)

4. (withdrawn): A semiconductor memory device according to claim 2, wherein

a connection surface of the storage electrode, which are connected to the first diffused region, is substantially parallel with a surface of the storage electrode, which correspond to the connection surface.

5. (currently amended): A semiconductor memory device comprising:

a device layer including

a semiconductor layer having a first diffused region and a second diffused region formed therein[[,]] and having substantially flat surfaces, said semiconductor layer defining a first side and a second side;

a transistor having a gate electrode formed ~~through an insulation film~~ only on [[one]] said first side of the semiconductor layer between the first and the second diffused regions[[,]] with an insulation film interposed therebetween; and

a capacitor formed only on said [[one]] first side of the semiconductor layer and having a storage electrode connected to the first diffused region;

a bit line formed on ~~the other~~ said second side of the semiconductor layer, and extended in a direction normal to the gate electrode; and

a support substrate formed on said [[one]] first side of the semiconductor layer for supporting the device layer;

the semiconductor layer including a first region which is extended in the extending direction ~~of extension~~ of the bit line and includes the first diffused region and the second diffused region, and a second region which is ~~extended in a direction of extension~~ adjacent to the first

region on a side of an extending direction of the gate electrode ~~in the first region~~ and includes the second diffused region;

a first contact hole being formed in the first region for connecting the first diffused region to the capacitor; and

a second contact hole being formed in the second region for connecting the bit line with the second diffused region.

6. (original): A semiconductor memory device according to claim 5, wherein

the first region and the second region are connected with each other.

7. (withdrawn): A semiconductor memory device according to claim 5, wherein

the second diffused region in the first region and the second diffused region in the second region are formed spaced from each other.

8. (withdrawn): A semiconductor memory device according to claim 6, further comprising

a first wiring layer formed on said one side of the semiconductor layer for connecting the first and the second regions with each other.

9. (withdrawn): A semiconductor memory device according to claim 7, further comprising

a first wiring layer formed on said one side of the semiconductor layer for connecting the first and the second regions with each other.

10. (currently amended): A semiconductor memory device according to claim 5, further comprising

a ~~scrapping~~ strapping word line formed on said [[other]] second side of the semiconductor layer and connected to the gate electrode.

11. (currently amended): A semiconductor memory device according to claim 5, further comprising

a ~~scrapping~~ strapping word line formed on said [[one]] first side of the semiconductor layer and connected to the gate electrode.

12. (original): A semiconductor memory device according to claim 5, further comprising

a shield electrode formed on the bit line for suppressing interference between the bit lines.

13. (canceled)

14. (original): A semiconductor memory device according to claim 5, wherein

the bit line is electrically connected to a region of the semiconductor layer between the first and the second diffused regions.

15-28. (canceled)

29. (withdrawn): A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed therein and having substantially flat surfaces, said silicon layer defining a first side and a second side;

a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a strapping word line formed on said second side of the silicon layer and connected to the gate electrode.

30. (withdrawn): A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed therein and having substantially flat surfaces, said silicon layer defining a first side and a second side;

a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a strapping word line formed on said first side of the silicon layer and connected to the gate electrode.

31. (withdrawn): A semiconductor memory device comprising:

a device layer including:

a silicon layer having a first diffused region and a second diffused region formed therein and having substantially flat surfaces, said silicon layer defining a first side and a second side;

a gate electrode formed only on said first side of the silicon layer between the first diffused region and the second diffused region interposing a gate insulating film between the gate electrode and the silicon layer;

a contact electrode formed on said first side of the silicon layer and connected to the second diffused region; and

a capacitor formed only on said first side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said second side of the silicon layer and electrically connected to the second diffused region via the contact electrode;

a support substrate formed on said first side of the silicon layer for supporting the device layer interposing an insulating film between the support substrate and the device layer; and

a shield electrode formed above the bit line for suppressing interference between the bit lines.